LISTING OF CLAIMS

1-20. (Canceled)

21. (Currently amended) A method of enhancing carrier mobility in a semiconductor active region of a semiconductor device having a predetermined channel type of either n-channel type or p-channel type, comprising:

selecting an appropriate one of compressive stress or tensile stress that when exerted on the active region will enhance carrier mobility within the active region for the channel type of the semiconductor device;

providing a layer of semiconductor material; and

providing a trench isolation region in the layer of semiconductor region that defines placement of the active region, the trench isolation region defined by sidewalls and a bottom and the providing the trench isolation region includes:

providing a liner that exerts the selected one of compressive stress or tensile stress on the active region, the liner made from a material having a relative permittivity (K) of about 10 or more and ~~, the liner~~ conforming to the sidewalls and bottom; and

providing a fill section made from isolating material that is disposed within and conforms to the liner ~~; and~~

~~exerting a selected one of compressive stress or tensile stress on the active region with the liner to enhance carrier mobility within the active region~~.

22. (Previously presented) The method according to claim 21, further comprising forming the semiconductor device using an active region and wherein the liner exerts compressive stress to compress the active region, the compressive stress effective to enhance electron mobility within the active region.

23. (Previously presented) The method according to claim 22, wherein the semiconductor device is an NMOS device.

24. (Previously presented) The method according to claim 21, further comprising forming the semiconductor device using an active region and wherein the liner exerts tensile stress to strain the active region, the tensile stress effective to enhance hole mobility within the active region.

25. (Previously presented) The method according to claim 24, wherein the semiconductor device is a PMOS device.

26. (Previously presented) The method according to claim 21, wherein the fill section is composed of one or more materials selected from silicon oxide, silicon nitride, polysilicon and mixtures thereof.

27. (Previously presented) The method according to claim 26, wherein the fill section is deposited using chemical vapor deposition (CVD).

28. (Previously presented) The method according to claim 21, wherein the layer of semiconductor material is a semiconductor film disposed on an insulating layer, the insulting layer being disposed on a semiconductor substrate.

29. (Previously presented) The method according to claim 28, wherein the bottom of the trench is defined by the insulating layer.

30. (Previously presented) The method according to claim 21, wherein the liner has a relative permittivity (K) of about 20 or more.